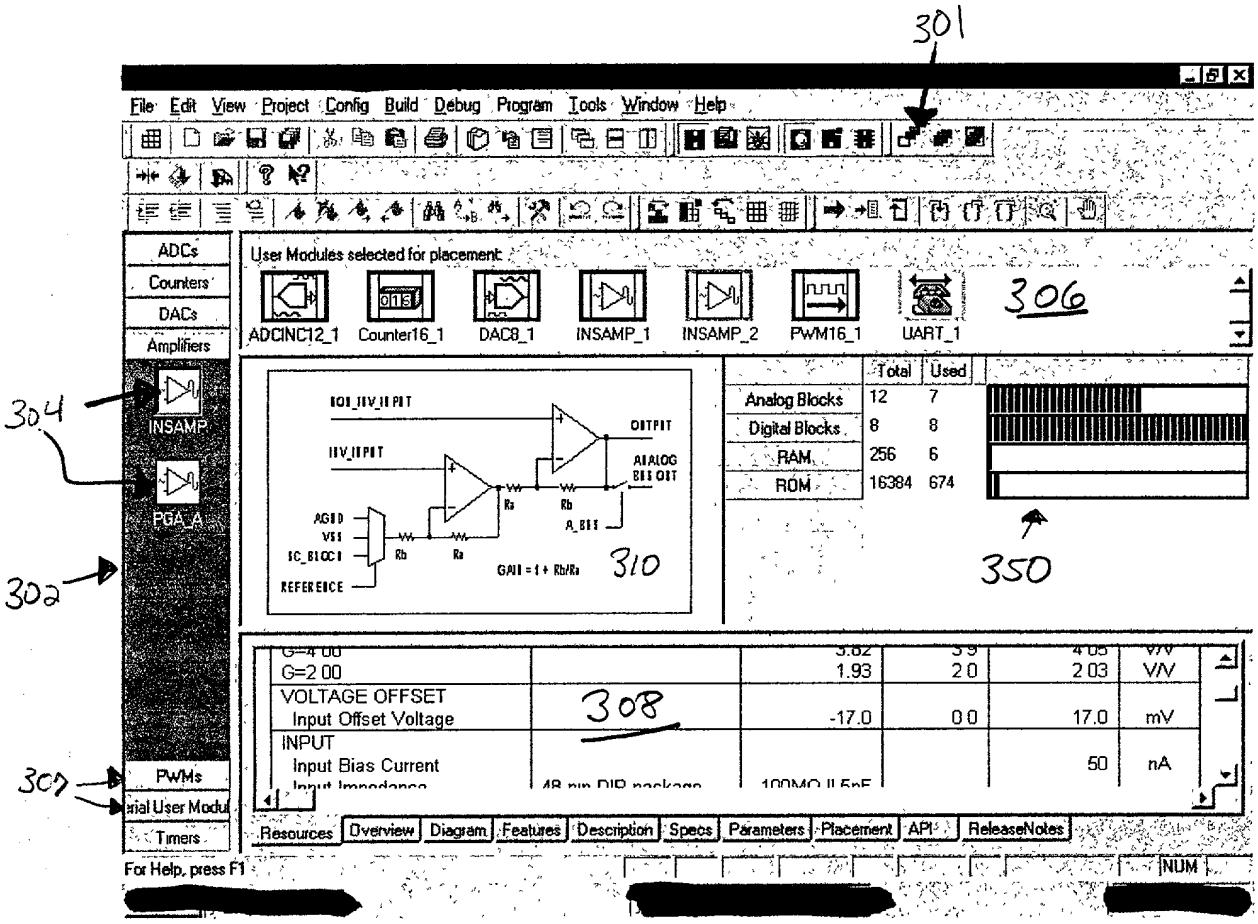

301
File Edit View Project Config Build Debug Program Tools Window Help
ADCs
Counters
DACs
Amplifiers
INSAMP
PGA_A
PWMs
Timers
User Modules selected for placement:
ADCINC12_1
Counter16_1
DAC8_1
INSAMP_1
INSAMP_2
PWM16_1
UART_1
306
304
302
307
310
Total
Used
Analog Blocks 12 7
Digital Blocks 8 8
RAM 256 6
ROM 16384 674
350
G=2.00 1.93 2.0 2.03 V/V
VOLTAGE OFFSET
Input Offset Voltage -17.0 0.0 17.0 mV
INPUT
Input Bias Current 50 nA
308
Resources
Overview
Diagram
Features
Description
Specs
Parameters
Placement
API
ReleaseNotes
For Help, press F1
NUM

Fig. 1A

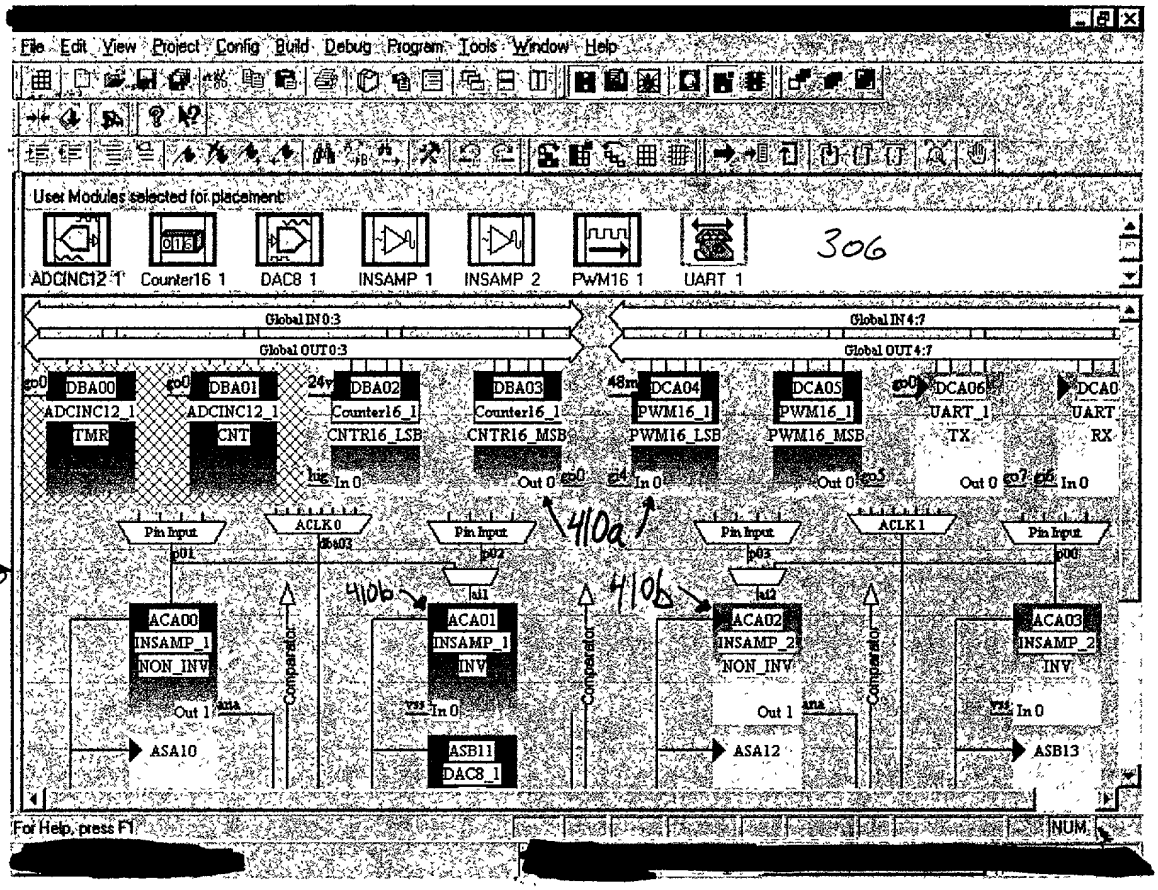

File Edit View Project Config Build Debug Program Tools Window Help
User Modules selected for placement:
ADCINC12_1
Counter16_1
DAC8_1
INSAMP_1
INSAMP_2
PWM16_1
UART_1
306
Global IN 0:3
Global IN 4:7
Global OUT 0:3
Global OUT 4:7
DBA00
ADCINC12_1
TMR
DBA01
ADCINC12_1
CNT
DBA02
Counter16_1
CNTR16_LSB
DBA03
Counter16_1
CNTR16_MSB
DCA04
PWM16_1
PWM16_LSB
DCA05
PWM16_1
PWM16_MSB
DCA06
UART_1
TX
DCA0
UART
RX
Pin Input
ACLK 0
ACLK 1
410a
410b
410b
360
ACA00
INSAMP_1
NON_INV
ACA01
INSAMP_1
INV
ACA02
INSAMP_2
NON_INV
ACA03
INSAMP_2
INV
Comparator
ASA10
ASB11
DAC8_1
ASA12
ASB13
For Help, press F1
NUM

Fig 1B

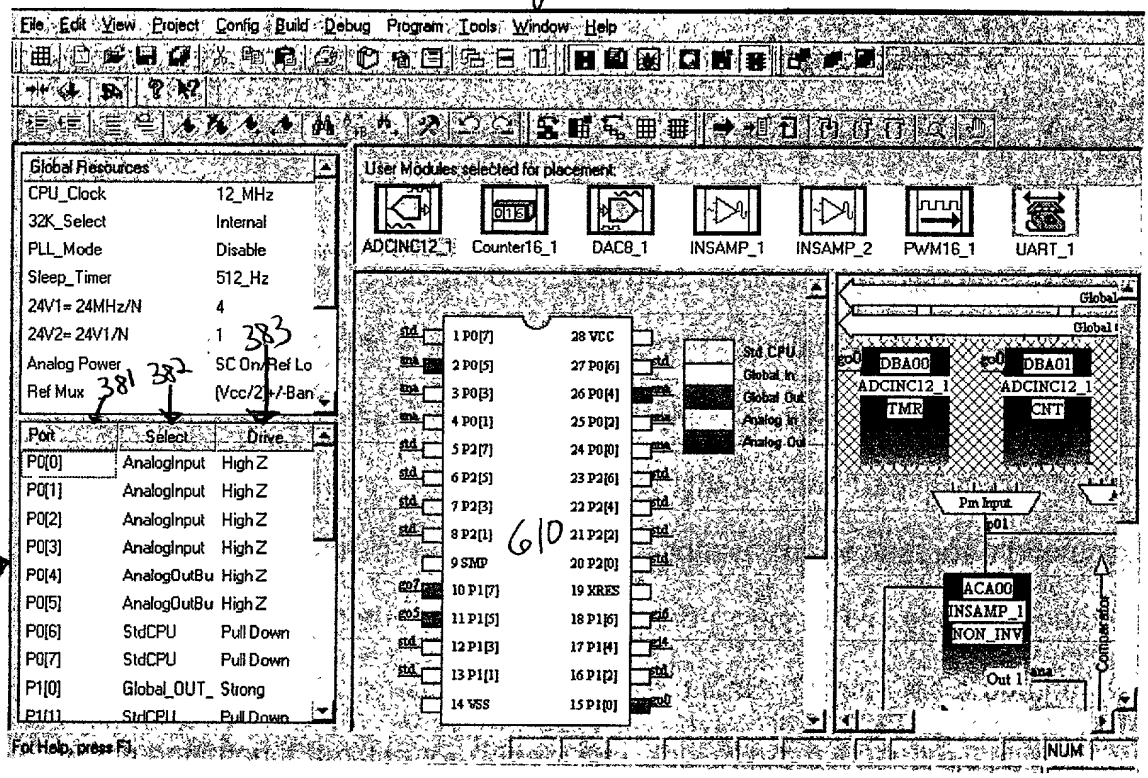

File Edit View Project Config Build Debug Program Tools Window Help
Global Resources
CPU_Clock 12_MHz
32K_Select Internal
PLL_Mode Disable
Sleep_Timer 512_Hz
24V1= 24MHz/N 4
24V2= 24V1/N 1
Analog Power SC On/Ref Lo
Ref Mux (Vcc/2+/-Ban
383
381
382
Port Select Drive
P0[0] AnalogInput HighZ
P0[1] AnalogInput HighZ
P0[2] AnalogInput HighZ
P0[3] AnalogInput HighZ
P0[4] AnalogOutBu HighZ
P0[5] AnalogOutBu HighZ
P0[6] StdCPU Pull Down
P0[7] StdCPU Pull Down
P1[0] Global_OUT_ Strong
P1[1] StdCPU Pull Down
380
User Modules selected for placement:
ADCINC12_1
Counter16_1
DAC8_1
INSAMP_1
INSAMP_2
PWM16_1
UART_1
1 P0[7]
2 P0[5]
3 P0[3]
4 P0[1]
5 P2[7]
6 P2[5]
7 P2[3]
8 P2[1]
9 SMP
10 P1[7]
11 P1[5]
12 P1[3]
13 P1[1]
14 VSS
28 VCC
27 P0[6]
26 P0[4]
25 P0[2]
24 P0[0]
23 P2[6]
22 P2[4]
21 P2[2]
20 P2[0]
19 XRES
18 P1[6]
17 P1[4]
16 P1[2]
15 P1[0]
610
Std CPU
Global In
Global Out
Analog In
Analog Out
Global
DBA00
ADCINC12_1
TMR
DBA01
ADCINC12_1
CNT
Pin Input
ACA00
INSAMP_1
NON_INV
Out 1
Comparator
For Help, press F1
NUM

Fig. 1C

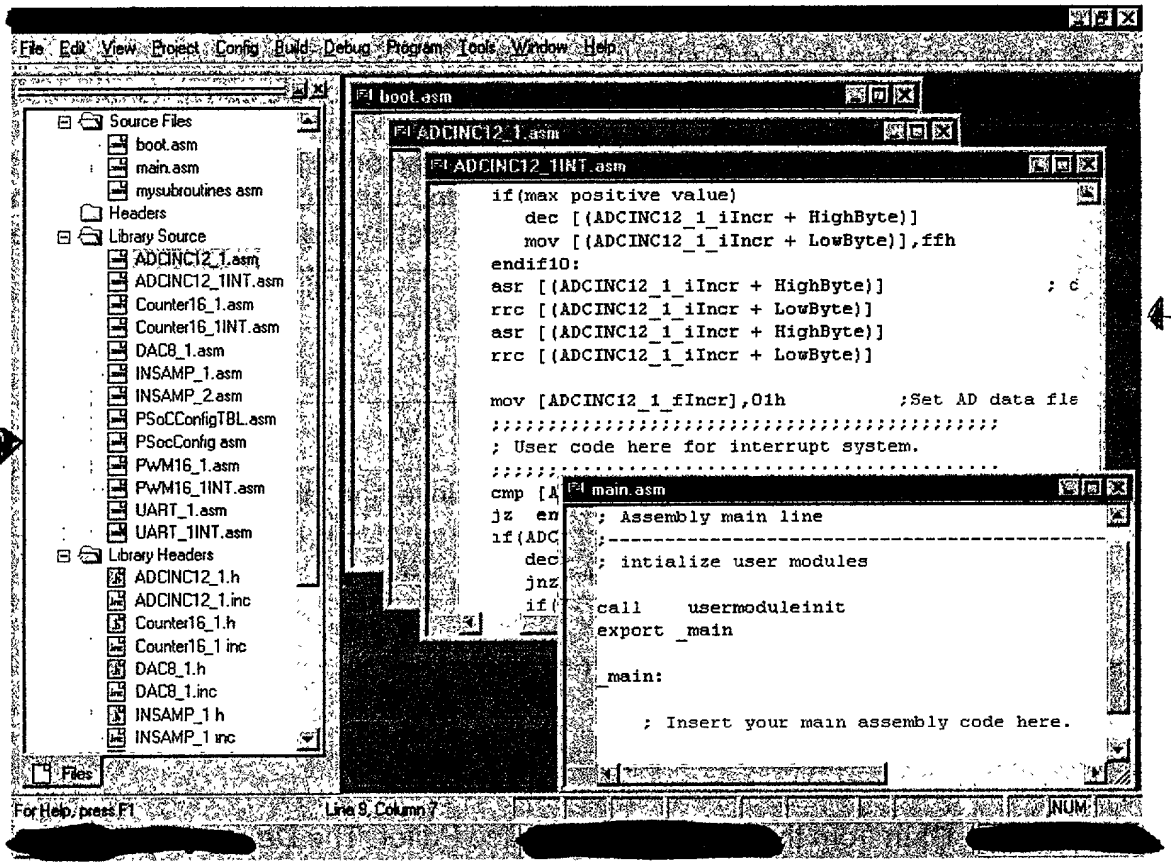

File Edit View Project Config Build Debug Program Tools Window Help
Source Files
boot.asm
main.asm
mysubroutines.asm
Headers
Library Source
ADCINC12_1.asm
ADCINC12_1INT.asm
Counter16_1.asm
Counter16_1INT.asm
DAC8_1.asm
INSAMP_1.asm
INSAMP_2.asm
PSoCConfigTBL.asm
PSocConfig.asm
PWM16_1.asm
PWM16_1INT.asm
UART_1.asm
UART_1INT.asm
Library Headers
ADCINC12_1.h
ADCINC12_1.inc
Counter16_1.h
Counter16_1.inc
DAC8_1.h
DAC8_1.inc
INSAMP_1.h
INSAMP_1.inc
Files
boot.asm
ADCINC12_1.asm
ADCINC12_1INT.asm
if(max positive value)
dec [(ADCINC12_1_iIncr + HighByte)]
mov [(ADCINC12_1_iIncr + LowByte)],ffh
endif10:
asr [(ADCINC12_1_iIncr + HighByte)]
rrc [(ADCINC12_1_iIncr + LowByte)]
asr [(ADCINC12_1_iIncr + HighByte)]
rrc [(ADCINC12_1_iIncr + LowByte)]
mov [ADCINC12_1_fIncr],01h ;Set AD data fla
; User code here for interrupt system.
main.asm
; Assembly main line
; intialize user modules
call usermoduleinit
export _main
_main:
; Insert your main assembly code here.
For Help, press F1
Line 9, Column 7
NUM
365
366

Fig. 1D

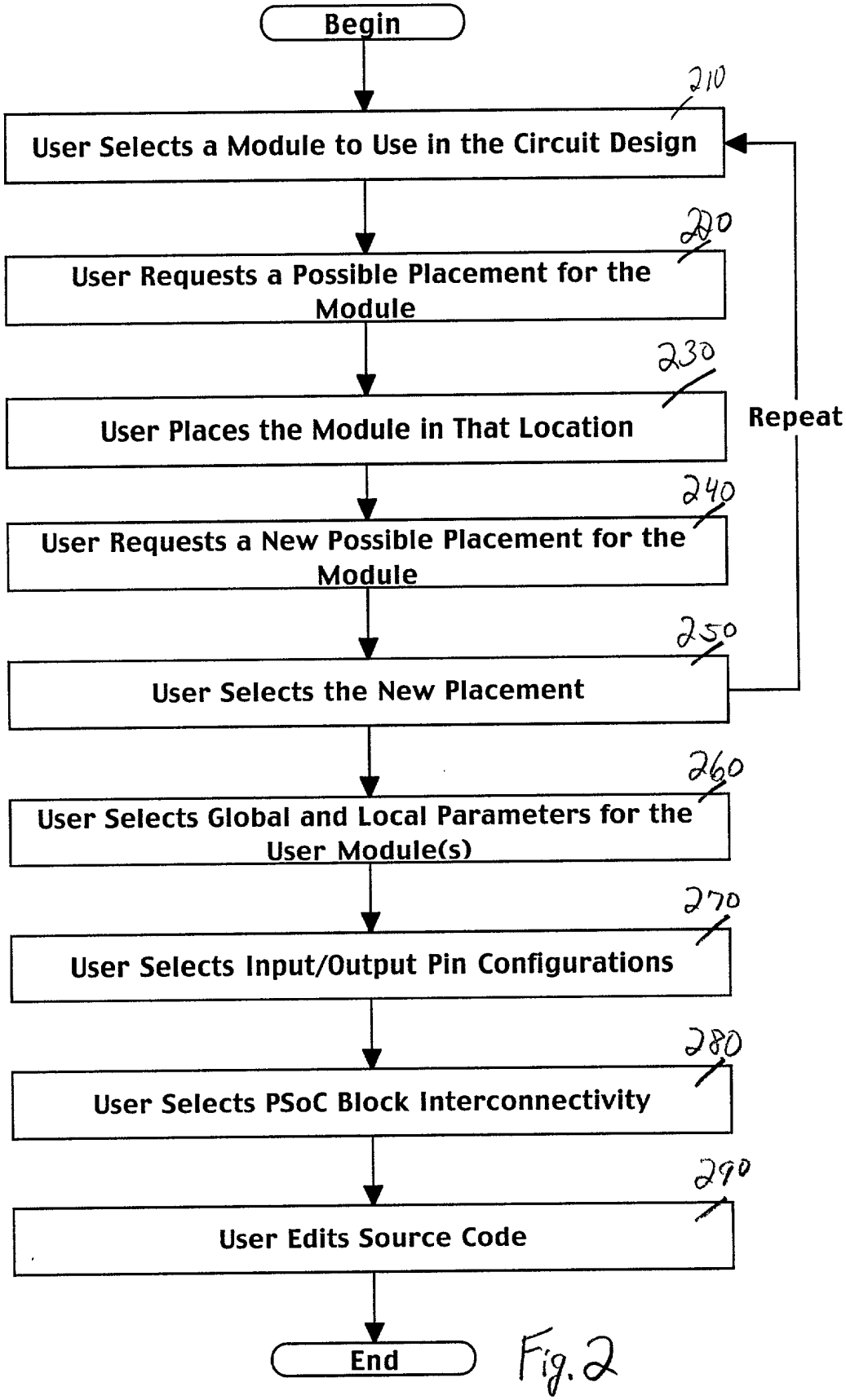
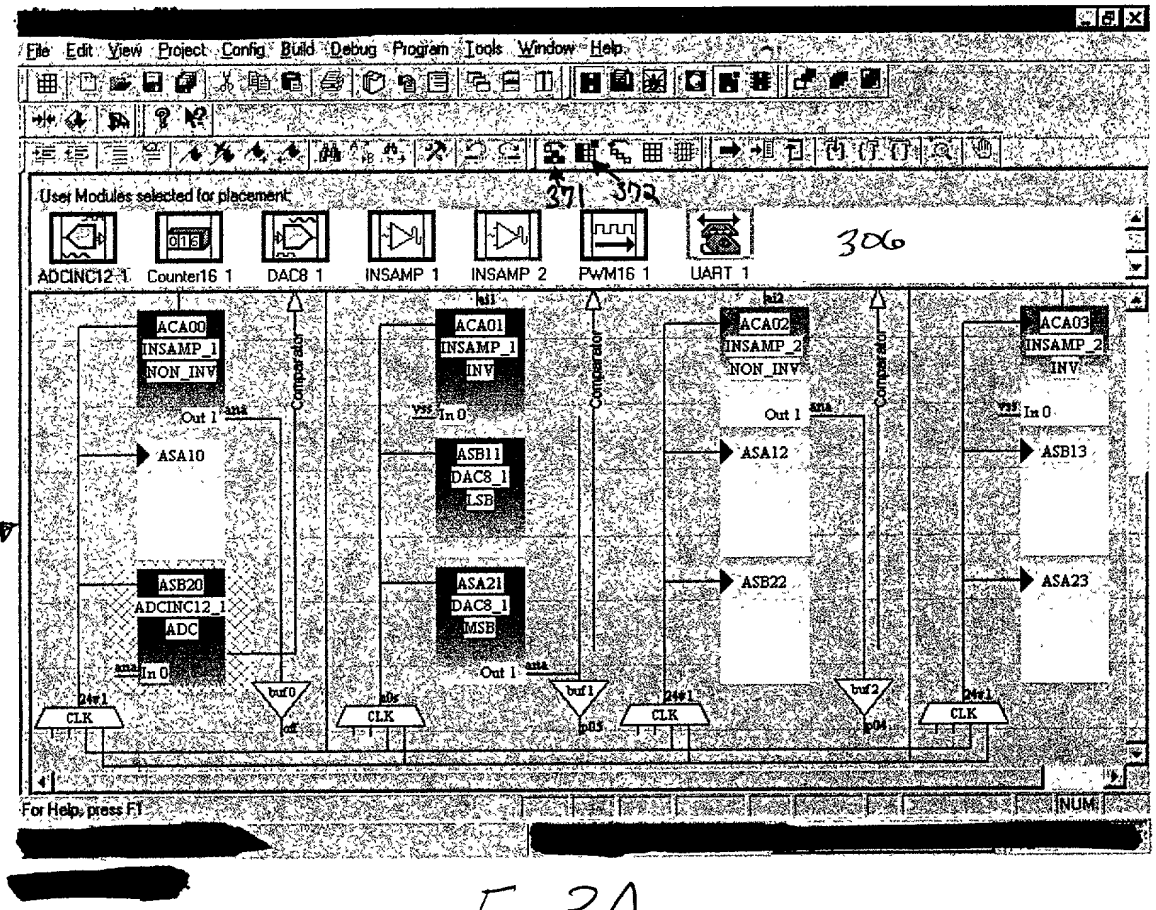

Begin
210
User Selects a Module to Use in the Circuit Design
220
User Requests a Possible Placement for the Module
230
User Places the Module in That Location
Repeat
240
User Requests a New Possible Placement for the Module
250
User Selects the New Placement
260
User Selects Global and Local Parameters for the User Module(s)
270
User Selects Input/Output Pin Configurations
280
User Selects PSoC Block Interconnectivity
290
User Edits Source Code
End

Fig. 2


File Edit View Project Config Build Debug Program Tools Window Help
User Modules selected for placement:
ADCINC12_1
Counter16_1
DAC8_1
INSAMP_1
INSAMP_2
PWM16_1
UART_1
306
ACA00
INSAMP_1
NON_INV
Out 1
ASA10
ASB20
ADCINC12_1
ADC
In 0
CLK
Comparator
buf0
ACA01
INSAMP_1
INV
In 0
ASB11
DAC8_1
LSB
ASA21
DAC8_1
MSB
Out 1
buf1
ACA02
INSAMP_2
NON_INV
Out 1
ASA12
ASB22
buf2
ACA03
INSAMP_2
INV
In 0
ASB13
ASA23
For Help, press F1
NUM

360

Fig. 3A

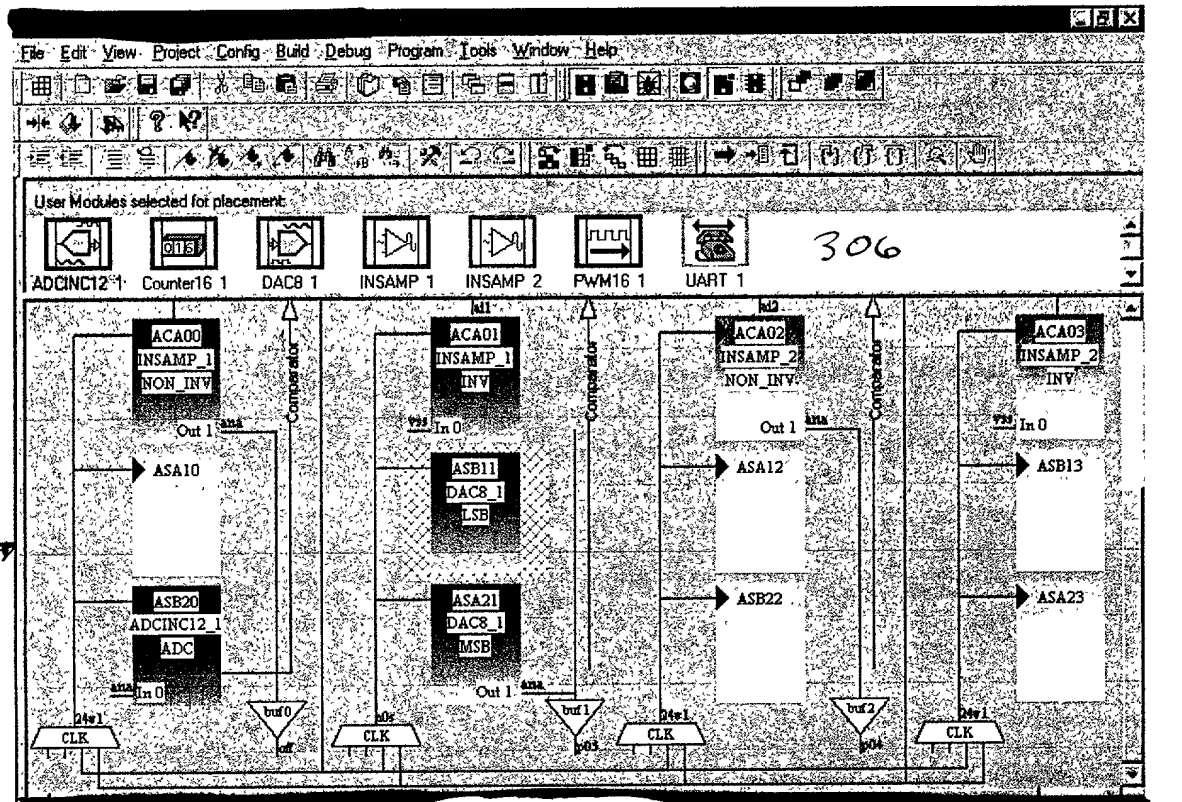

File Edit View Project Config Build Debug Program Tools Window Help
User Modules selected for placement:
ADCINC12_1
Counter16_1
DAC8_1
INSAMP_1
INSAMP_2
PWM16_1
UART_1
306
360
ACA00
INSAMP_1
NON_INV
ACA01
INSAMP_1
INV
ACA02
INSAMP_2
NON_INV
ACA03
INSAMP_2
INV
Comparator
Out 1
In 0
ASA10
ASB11
DAC8_1
LSB
ASA12
ASB13
ASB20
ADCINC12_1
ADC
ASA21
DAC8_1
MSB
ASB22
ASA23
CLK
buf0
buf1
buf2

FIG3B

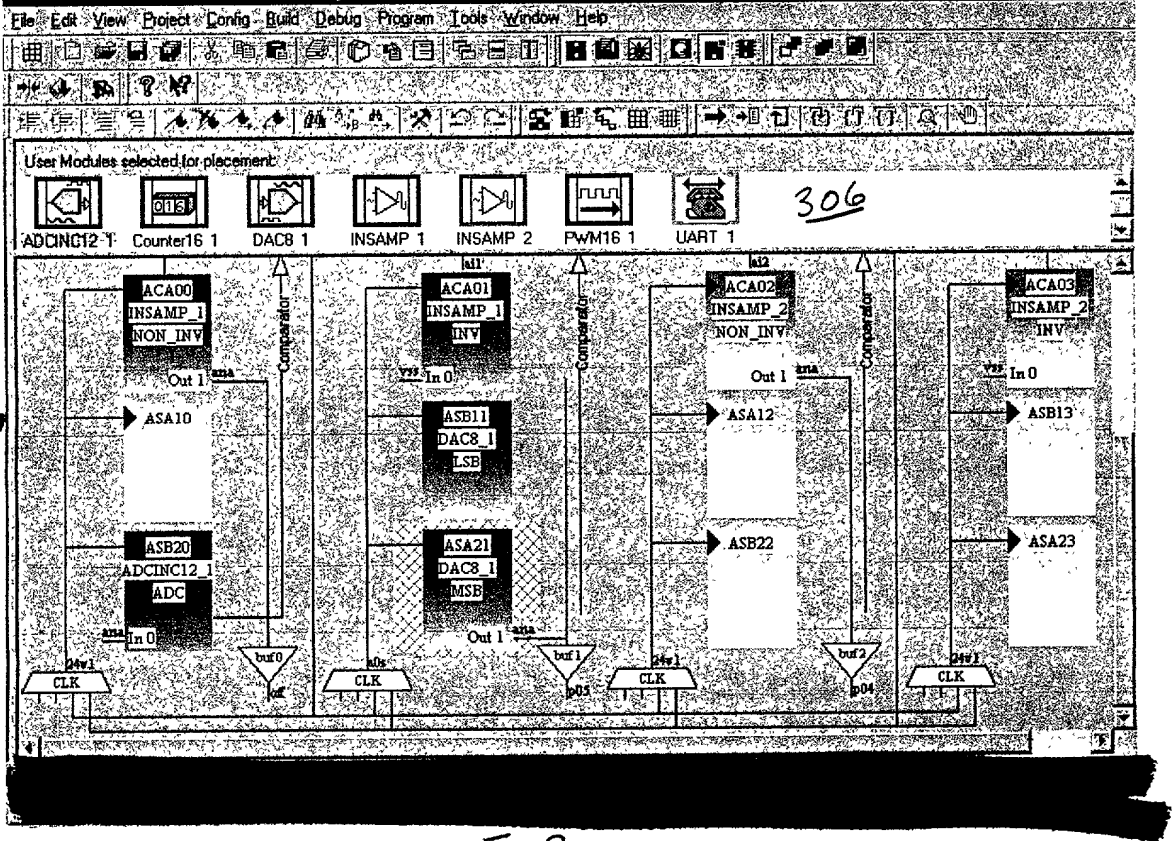

File Edit View Project Config Build Debug Program Tools Window Help
User Modules selected for placement:
ADCINC12_1
Counter16_1
DAC8_1
INSAMP_1
INSAMP_2
PWM16_1
UART_1
306
360
ACA00
INSAMP_1
NON_INV
ACA01
INSAMP_1
INV
ACA02
INSAMP_2
NON_INV
ACA03
INSAMP_2
INV
Comparator
Out 1
In 0
ASA10
ASB11
DAC8_1
LSB
ASA12
ASB13
ASB20
ADCINC12_1
ADC
ASA21
DAC8_1
MSB
ASB22
ASA23
CLK
buf0
buf1
buf2

Fig. 3C

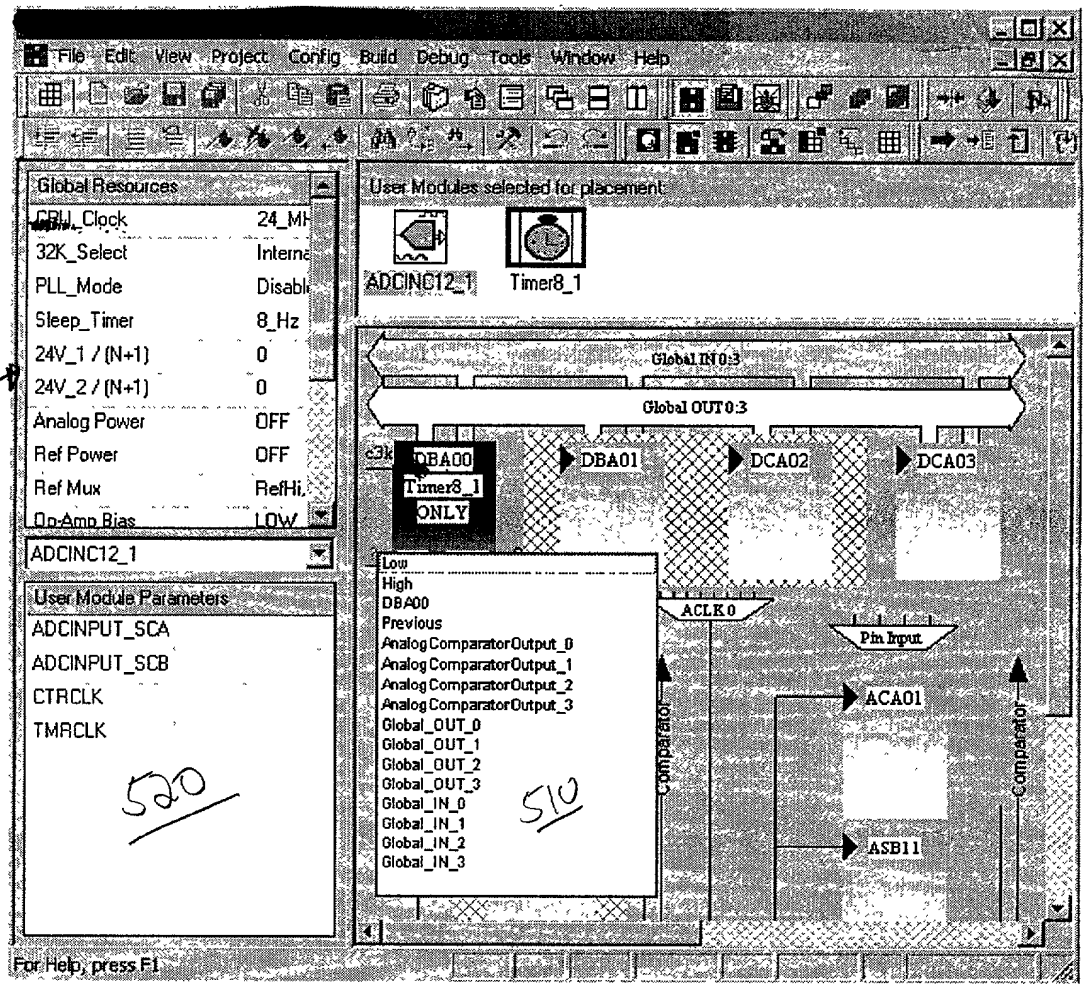

File Edit View Project Config Build Debug Tools Window Help
Global Resources
CPU_Clock 24_MH
32K_Select Interna
PLL_Mode Disabl
Sleep_Timer 8_Hz
24V_1 / (N+1) 0
24V_2 / (N+1) 0
Analog Power OFF
Ref Power OFF
Ref Mux RefHi
Op-Amp Bias LOW
ADCINC12_1
User Module Parameters
ADCINPUT_SCA
ADCINPUT_SCB
CTRCLK
TMRCLK
User Modules selected for placement
ADCINC12_1
Timer8_1
Global IN 0:3
Global OUT 0:3
DBA00
Timer8_1
ONLY
DBA01
DCA02
DCA03
Low
High
DBA00
Previous
Analog ComparatorOutput_0
Analog ComparatorOutput_1
Analog ComparatorOutput_2
Analog ComparatorOutput_3
Global_OUT_0
Global_OUT_1
Global_OUT_2
Global_OUT_3
Global_IN_0
Global_IN_1
Global_IN_2
Global_IN_3
ACLK 0
Pin Input
ACA01
ASB11
Comparator
Comparator
For Help, press F1
370
520
510

Fig. 4

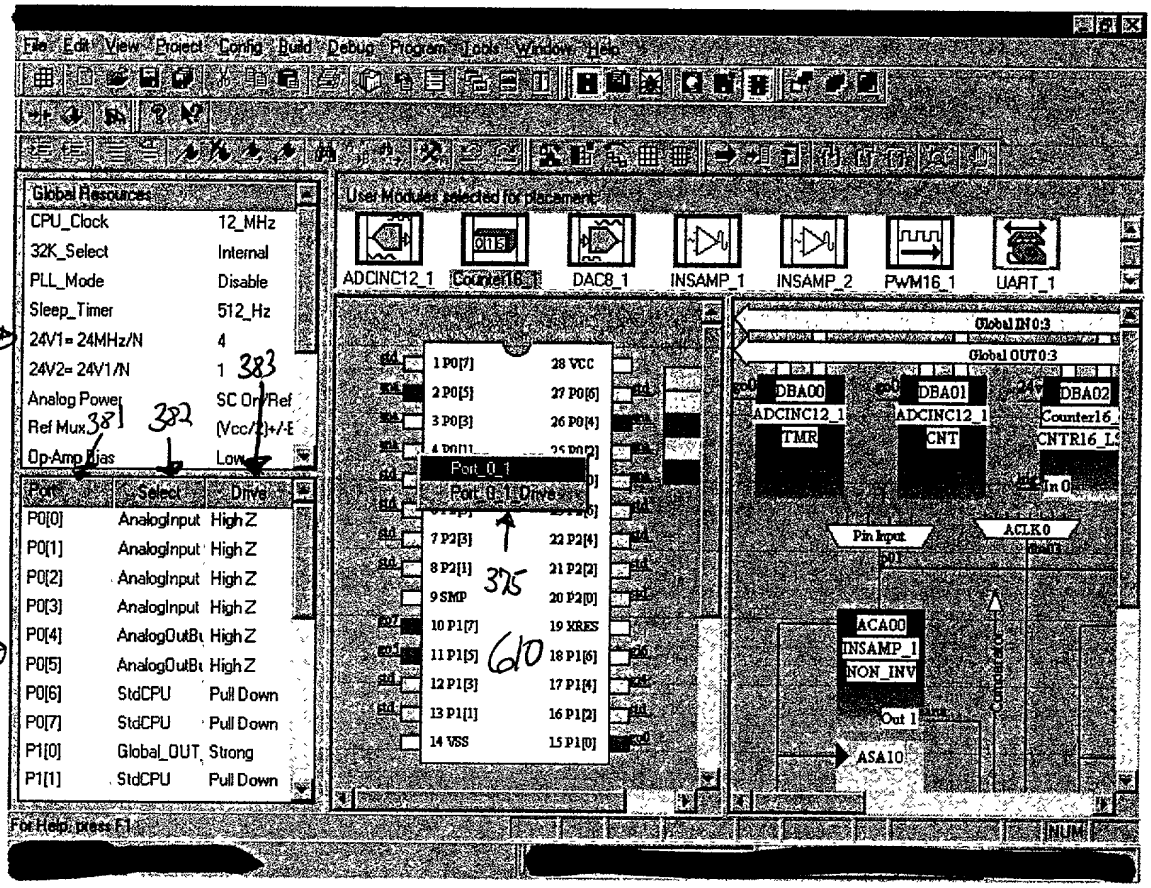
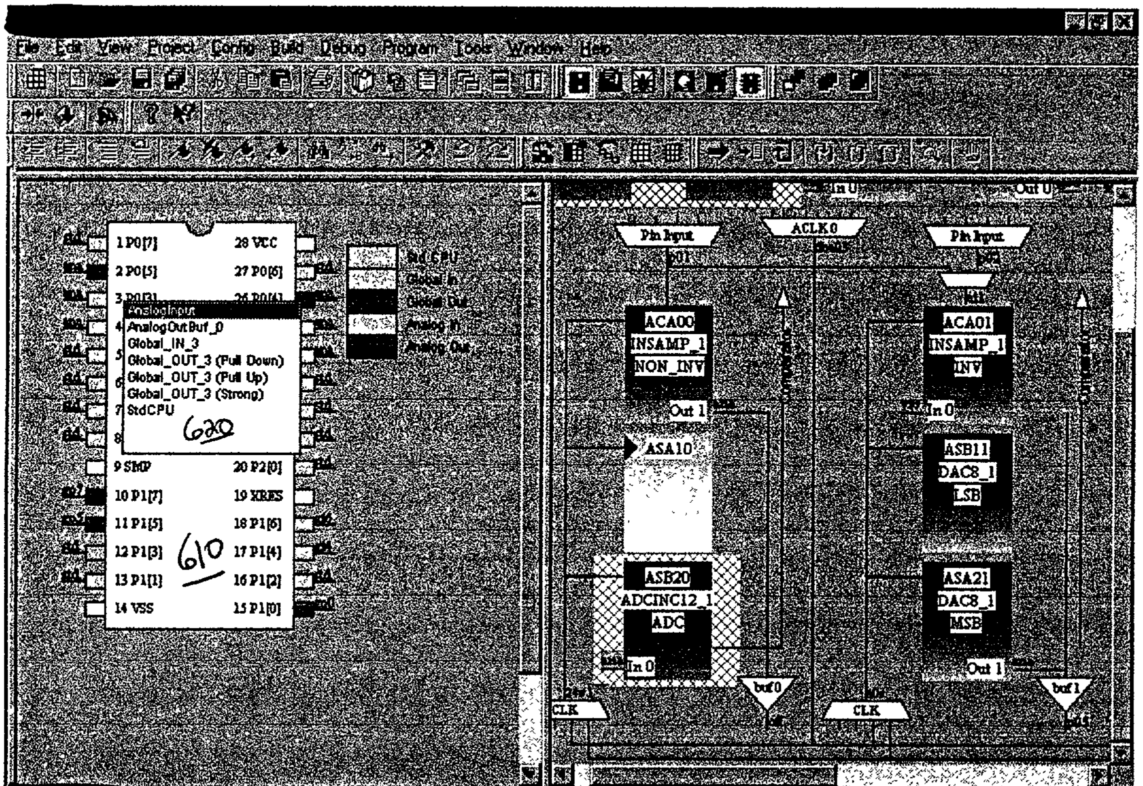
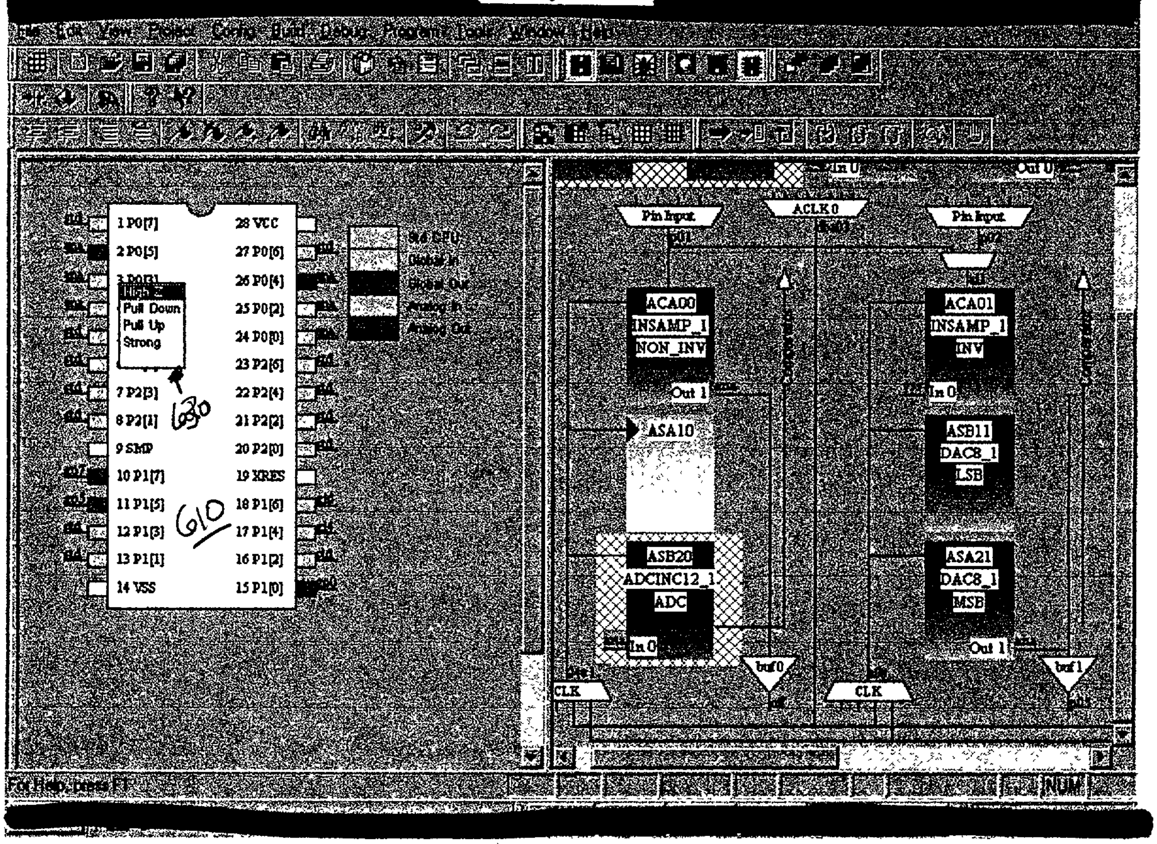

File Edit View Project Config Build Debug Program Tools Window Help
Global Resources
CPU_Clock 12_MHz
32K_Select Internal
PLL_Mode Disable
Sleep_Timer 512_Hz
24V1 = 24MHz/N 4
24V2 = 24V1/N 1
Analog Power SC On/Ref
Ref Mux (Vcc/2)+/-E
Op Amp Bias Low
Port Select Drive
P0[0] AnalogInput High Z
P0[1] AnalogInput High Z
P0[2] AnalogInput High Z
P0[3] AnalogInput High Z
P0[4] AnalogOutB High Z
P0[5] AnalogOutB High Z
P0[6] StdCPU Pull Down
P0[7] StdCPU Pull Down
P1[0] Global_OUT Strong
P1[1] StdCPU Pull Down
For Help, press F1
User Modules selected for placement:
ADCINC12_1
Counter16_1
DAC8_1
INSAMP_1
INSAMP_2
PWM16_1
UART_1
1 P0[7]
2 P0[5]
3 P0[3]
7 P2[3]
8 P2[1]
9 SMP
10 P1[7]
11 P1[5]
12 P1[3]
13 P1[1]
14 VSS
28 VCC
27 P0[6]
26 P0[4]
22 P2[4]
21 P2[2]
20 P2[0]
19 XRES
18 P1[6]
17 P1[4]
16 P1[2]
15 P1[0]
Port_0_1
Port_0_1 Drive
Global IN 0:3
Global OUT 0:3
DBA00
ADCINC12_1
TMR
DBA01
ADCINC12_1
CNT
DBA02
Counter16_
CNTR16_L
Pin Input
ACLK 0
ACA00
INSAMP_1
NON_INV
Out 1
ASA10
NUM
370
380
381
382
383
375
610

Fig. 5A


File Edit View Project Config Build Debug Program Tools Window Help
1 P0[7]
28 VCC
2 P0[5]
27 P0[6]
AnalogInput
AnalogOutBuf_0
Global_IN_3
Global_OUT_3 (Pull Down)
Global_OUT_3 (Pull Up)
Global_OUT_3 (Strong)
StdCPU
620
9 SMP
20 P2[0]
10 P1[7]
19 XRES
11 P1[5]
18 P1[6]
12 P1[3]
17 P1[4]
13 P1[1]
16 P1[2]
14 VSS
15 P1[0]
610
Pin Input
ACLK0
ACA00
INSAMP_1
NON_INV
ACA01
INV
Out 1
In 0
ASA10
ASB11
DAC8_1
LSB
ASB20
ADCINC12_1
ADC
ASA21
MSB
buf0
buf1
CLK
Fig. 5B


1 P0[7]
28 VCC
2 P0[5]
27 P0[6]
26 P0[4]
High Z
Pull Down
Pull Up
Strong
25 P0[2]
24 P0[0]
23 P2[6]
7 P2[3]
22 P2[4]
8 P2[1]
21 P2[2]
630
9 SMP
20 P2[0]
10 P1[7]
19 XRES
11 P1[5]
18 P1[6]
12 P1[3]
17 P1[4]
13 P1[1]
16 P1[2]
14 VSS
15 P1[0]
610
Pin Input
ACLK0
ACA00
INSAMP_1
NON_INV
ACA01
INV
Out 1
In 0
ASA10
ASB11
DAC8_1
LSB
ASB20
ADCINC12_1
ADC
ASA21
MSB
buf0
buf1
CLK
For Help, press F1
NUM
Fig. 5C

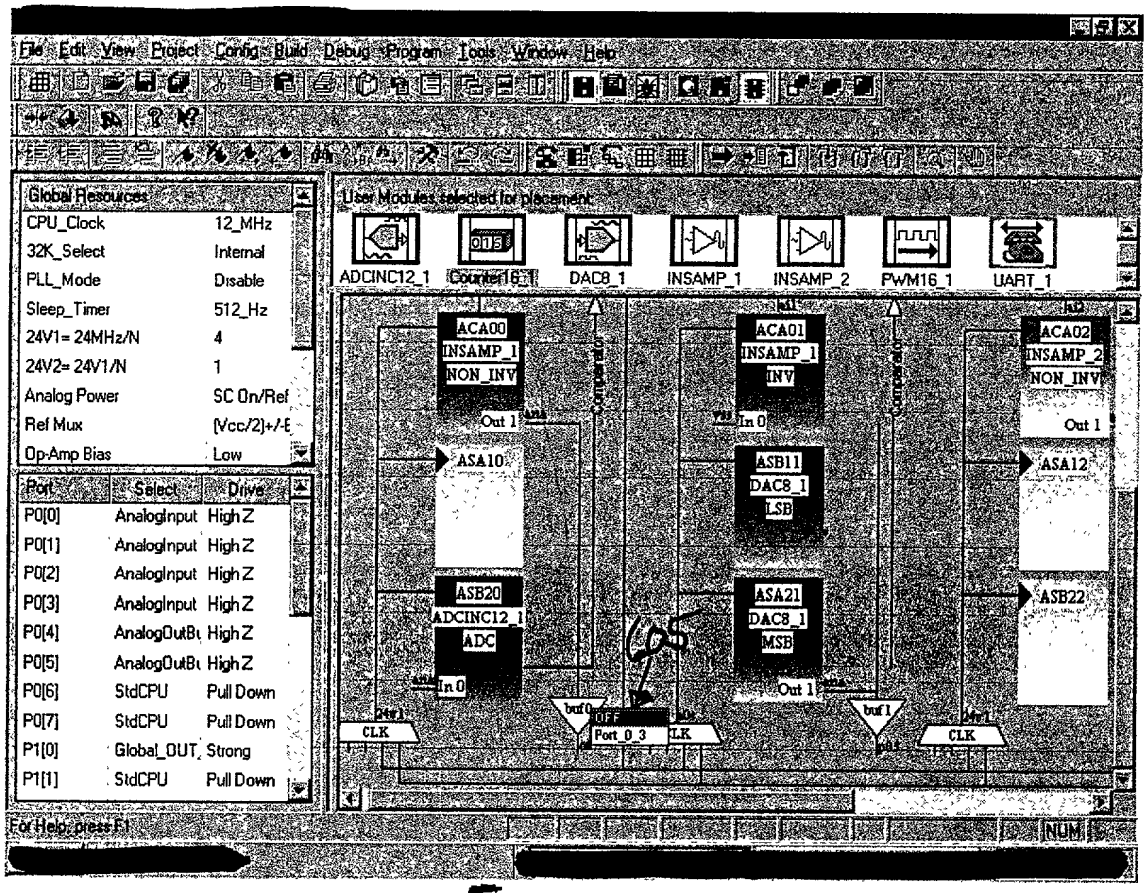
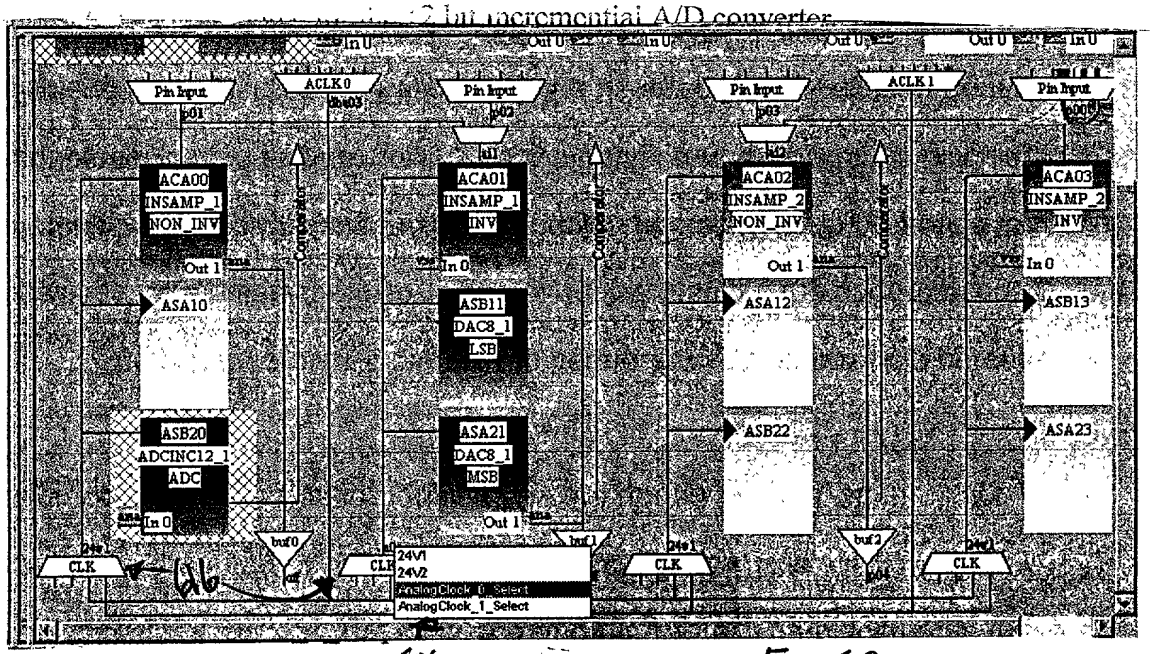


Fig. 6A



606

Fig. 6B

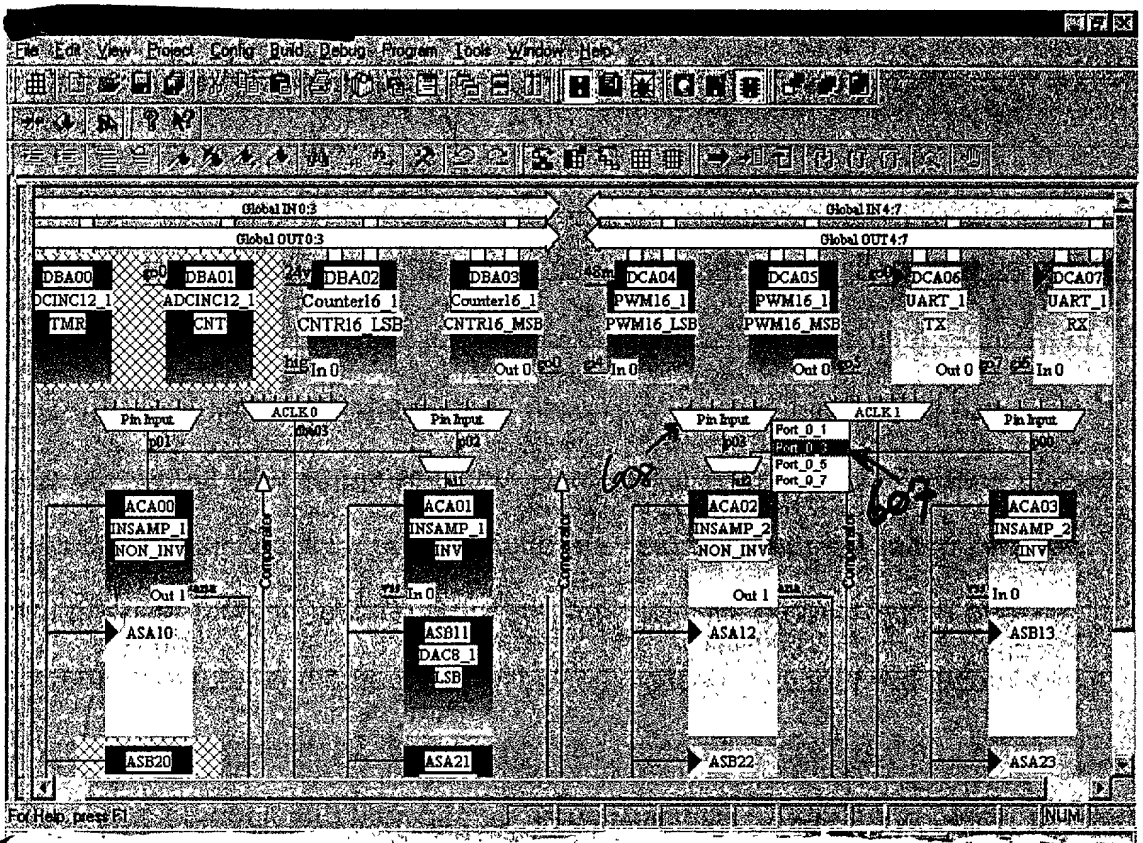

File Edit View Project Config Build Debug Program Tools Window Help
Global IN 0:3
Global IN 4:7
Global OUT 0:3
Global OUT 4:7
DBA00
DCINC12_1
TMR
DBA01
ADCINC12_1
CNT
DBA02
Counter16_1
CNTR16_LSB
DBA03
Counter16_1
CNTR16_MSB
DCA04
PWM16_1
PWM16_LSB
DCA05
PWM16_1
PWM16_MSB
DCA06
UART_1
TX
DCA07
UART_1
RX
Pin Input
ACLK 0
ACLK 1
Port_0_1
Port_0_3
Port_0_5
Port_0_7
ACA00
INSAMP_1
NON_INV
ACA01
INSAMP_1
INV
ACA02
INSAMP_2
NON_INV
ACA03
INSAMP_2
INV
ASA10
ASB11
DAC8_1
LSB
ASA12
ASB13
ASB20
ASA21
ASB22
ASA23
For Help, press F1
NUM

Fig.6C

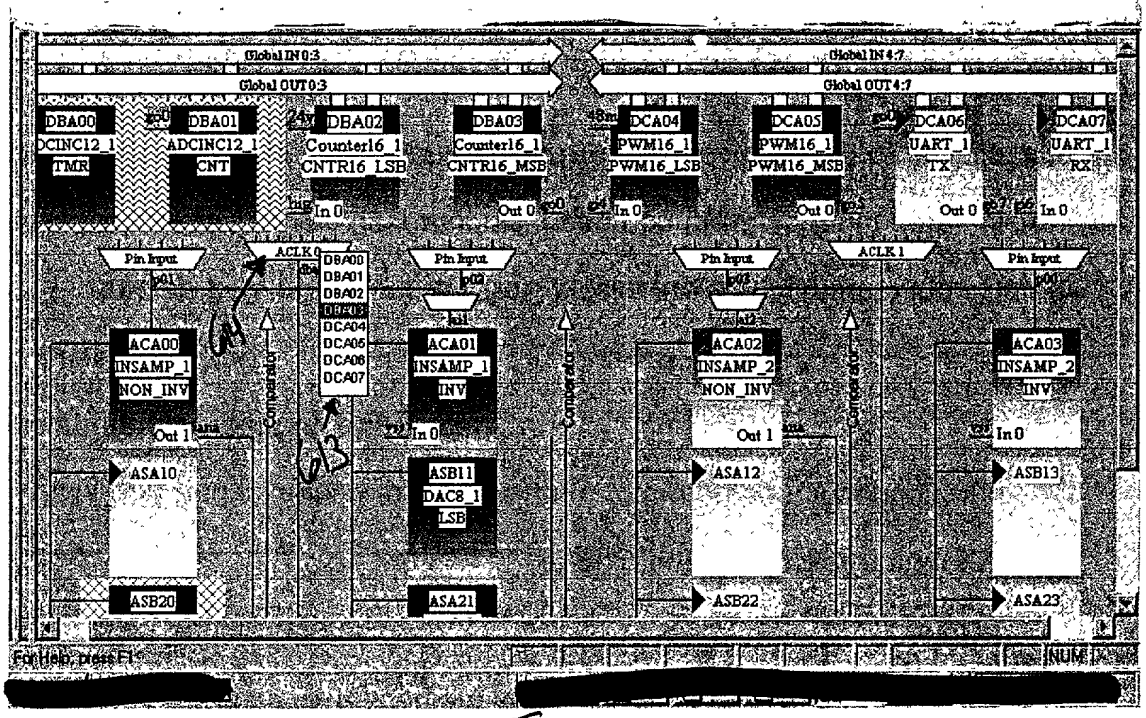

Global IN 0:3
Global IN 4:7
Global OUT 0:3
Global OUT 4:7
DBA00
DCINC12_1
TMR
DBA01
ADCINC12_1
CNT
DBA02
Counter16_1
CNTR16_LSB
DBA03
Counter16_1
CNTR16_MSB
DCA04
PWM16_1
PWM16_LSB
DCA05
PWM16_1
PWM16_MSB
DCA06
UART_1
TX
DCA07
UART_1
RX
Pin Input
ACLK 0
ACLK 1
DBA00
DBA01
DBA02
DBA03
DCA04
DCA05
DCA06
DCA07
ACA00
INSAMP_1
NON_INV
ACA01
INSAMP_1
INV
ACA02
INSAMP_2
NON_INV
ACA03
INSAMP_2
INV
ASA10
ASB11
DAC8_1
LSB
ASA12
ASB13
ASB20
ASA21
ASB22
ASA23
For Help, press F1
NUM

Fig.6D